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10/776,358	02/11/2004	Patrick Wai-Tong Leung	VP095	3213

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,358	LEUNG ET AL.	
	Examiner	Art Unit	
	Katrina Fujita	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39,42,45 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39, 42, 45 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is responsive to Applicant's remarks received on June 29, 2007. Claims 1-39, 42, 45 and 46 remain pending.

Specification

2. The previous specification objections have been withdrawn in light of applicant's amendment.

Claim Objections

3. The following is a quotation of 37 CFR 1.75(d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

4. Claims 1, 12, 24 and 35 are objected to under 37 CFR 1.75(d)(1), as failing to conform to the invention as set forth in the remainder of the specification.

Claim 1 recites "(N – M)+/- 1 pixels of the image data are sampled" in line 5. However, in the specification on page 11, line 4, it states "(N – M) pixels are dropped

out of every N pixels". Therefore, the specification does not provide "clear support or antecedent basis in the description" for sampling (N – M) pixels. The same applies to claim 12, line 4, claim 24, line 6 and claim 35, line 8. Correction or clarification is required.

Claim 1 recites "N/M downscaling" in line 1. However, in the specification on page 11, line 5, it states "M/N scaling". Therefore, the specification does not provide "clear support or antecedent basis in the description" for N/M scaling. It appears that this was a typographical error and will be assumed as the following for examination purposes: -- M/N downscaling --. The same applies to claim 12, line 1.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-6, 8-18, 20-22, 24-29, and 31-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Boehlke et al. (US 5,862,268).

Regarding **claims 1, 12 and 24** Boehlke et al. discloses a method, an apparatus, and a medium readable by a machine embodying a program of instructions executable by the machine to perform a method for M/N downscaling digital image data ("the decimator computes a preliminary output sequence Y(n,h) by implementing the following algorithm (expressed in pseudocode): " at col. 3, line 28) comprising,

a sampling circuit (figure 4, numeral 26; figure 5) for sampling a sequence of image data ("bilinear decimator 26 of FIG. 4 which converts the input data sequence...into the output data sequence" at col. 5, line 64), the sequence corresponding to one dimension of a rectangular array of image data and having R pixels (figure 1) so that (N - M) +/- 1 pixels of the image data are sampled for every N pixels of said sequence ("a 'decimation ratio P/N'. Thus decimator 26 knows the required relationship between the number of high and low resolution image lines" at col. 5, line 45; in the case where the ratio is the output will accordingly have (2 –1) = 1 output pixel for every 2 input pixels), where R, M and N are integers, N < R and M < N ("number of line P in the low resolution image" at col. 6, line 3; "number of lines N in the high resolution image" at col. 5, line 44).

Regarding **claim 2**, Boehlke et al. discloses a graphics display device (figure 4, numeral 22) for displaying the sampled said image data ("video conversion system converts the video output of source 20 to another video signal suitable for driving a different kind of display monitor 22" at col. 5, line 27).

Regarding **claims 3 and 5,** Boehlke et al. discloses an adding circuit (figure 5, numeral 40) for creating a count sequence corresponding to said sequence of image data ("Adder 40a, having a count limit N" at col. 6, line 32), wherein said sampling circuit is adapted for determining whether a particular count of said count sequence is less than N ("Adder 40a overflows upon counting to N, and generates the overflow signal" at col. 6, line 42), and if true, selecting a corresponding instance of image data ("A sequencer 30, clocked by a LOAD signal generated by decimator 26 whenever it produces a valid output data value Y(p,h), sequentially addresses and write enables an input port of a two-port memory 28" at col. 5, line 50).

Regarding **claims 4, 14, 17, 26, and 28,** Boehlke et al. discloses an apparatus further comprising creating a count sequence corresponding to said sequence of image data ("Adder 40a, having a count limit N" at col. 6, line 32), wherein said sampling circuit is adapted for determining whether an instance of said count sequence is less than N ("Adder 40a overflows upon counting to N, and generates the overflow signal" at col. 6, line 42), and if true, selecting a corresponding instance of image data ("A sequencer 30, clocked by a LOAD signal generated by decimator 26 whenever it produces a valid output data value Y(p,h), sequentially addresses and write enables an input port of a two-port memory 28" at col. 5, line 50).

Regarding **claims 6, 8, 9, 15, 18, 20, 21, 29, 31, and 32,** Boehlke et al. discloses an apparatus wherein said adding circuit includes an n-bit adder (figure 5, numeral 40a, where 40a is a 1-bit adder), where $N = 2^n$, n is a positive integer (in the case where N =

2, n =1), and wherein said sampling circuit is adapted to sample (N – M) of said pixels for every N pixels of said sequence.

Regarding **claims 10 and 33**, Boehlke et al. discloses an apparatus wherein M is greater than 1 (it is also surmised that the case of N = 3 and M = 2 is anticipated as for every 3 pixels of data input, (3-2)+1 = 2 pixels are output).

Regarding **claim 13, and 25**, Boehlke et al. discloses a graphics display device for displaying the sampled said image data ("driving display monitor 22 so that it produces the lower resolution image" at col. 5, line 62).

Regarding **claims 16 and 22**, Boehlke et al. discloses that said n-bit adder counts in increments of N-M (in this case, counts in increments of 1).

Regarding **claim 27**, Boehlke et al. discloses an apparatus further comprising creating a count sequence corresponding to said sequence of image data ("Adder 40a, having a count limit N" at col. 6, line 32) in which said count sequence is incremented in steps of N-M (in this case, counts in increments of 1), wherein said sampling circuit is adapted for determining whether an instance of said count sequence is less than N ("Adder 40a overflows upon counting to N, and generates the overflow signal" at col. 6, line 42), and if true, selecting a corresponding instance of image data ("A sequencer 30, clocked by a LOAD signal generated by decimator 26 whenever it produces a valid output data value Y(p,h), sequentially addresses and write enables an input port of a two-port memory 28" at col. 5, line 50).

Regarding **claims 11, 23, and 34**, Boehlke et al. discloses creating two or more count sequences, each count sequence corresponding to said sequence of image data,

wherein a first count sequence counts to a first count value N1 (figure 5, numeral 40a) and a second count sequence counts to a second count value N2 (figure 5, numeral 41), and wherein when one of said two or more count sequences counts to its respective count value, a corresponding instance of image data is not sampled ("Adder 40a overflows upon counting to N, and generates the overflow signal OF(n+1). On the next NEW LINE pulse, C(n) is reset to a low value and the OF(n) signal is asserted" at col. 6, line 42).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7, 19 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Boehlke et al. and Crean et al. (US 5,745,249).

Boehlke et al. discloses an adding circuit adapted to begin a count sequence as described in the 102 rejections above.

Boehlke et al. does not disclose beginning said count sequence at an offset K.

Crean et al. discloses an image processing system beginning a count sequence ("functional requirements of sequencer 40 are that it be able to initialize at the beginning

of a scan line, start at an offset location in memory representing an offset within the brick" at col. 6, line 31) at an offset K ("precomputed brick parameters (e.g., offset within the brick)" at col. 6, line 36; figure 1, letter S).

It would have been obvious at the time the invention was made to one of ordinary skill in the art for the count sequence of Boehlke et al. to be shifted using the offset taught by Crean et al. as described above, to "support the requirements of, for example, process controls, customer selection, and/or object optimized rendering" (Crean et al., at col.6, line 17).

9. Claims 35, 37-39, 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Boehlke et al. and Acharya (US 6,215,916).

Regarding **claim 35**, Boehlke et al. discloses a system for displaying images, comprising a host ("video source 20, such as for example a computer" at col. 5, line 23), a graphics display device, and a graphics controller that includes a sampling circuit to sample (figure 5) a sequence of image data, the sequence corresponding to one dimension of a rectangular array of image data and having R pixels wherein (N - M) +/- 1 pixels of the image data are sampled for every N pixels of said sequence, where R, M and N are integers, $N < R$ and $M < N$.

Boehlke et al. does not disclose a camera.

Acharya discloses a system for displaying images (figure 7) comprising a camera as the video source (figure 7, numeral 730; "Camera 730 may be a digital camera, digital video camera, or any image capture device" at col. 12, line 17).

It would have been obvious at the time the invention was made to one of ordinary skill in the art for the image data of Boehlke et al. to be supplied by the camera taught by Acharya as described above, such that the image data can be "quickly processed and transmitted" (Acharya, at col. 12, line 34).

Regarding **claims 37 and 40**, Boehlke et al. discloses a sampling circuit wherein said sampling circuit further comprises an adding circuit (figure 5, numeral 40) to create a count sequence corresponding to said sequence of image data ("Adder 40a, having a count limit N" at col. 6, line 32), wherein said sampling circuit is adapted to determine whether a particular count of said count sequence is less than N ("Adder 40a overflows upon counting to N, and generates the overflow signal" at col. 6, line 42), and if true, to select a corresponding instance of image data ("A sequencer 30, clocked by a LOAD signal generated by decimator 26 whenever it produces a valid output data value Y(p,h), sequentially addresses and write enables an input port of a two-port memory 28" at col. 5, line 50).

Regarding **claim 38**, Boehlke et al. discloses an apparatus wherein said adding circuit includes an n-bit adder (figure 5, numeral 40a, where 40a is a 1-bit adder), $N = 2^n$, n is a positive integer (in the case where N = 2, n =1), and wherein said sampling circuit samples (N – M) of said pixels for every N pixels of said sequence.

Regarding **claim 39**, Boehlke et al. discloses that said n-bit adder counts in increments of N-M(in this case, counts in increments of 1).

Regarding **claim 45**, Boehlke et al. discloses a system wherein said system transmits the sampled said image data ("video conversion system converts the video output of source 20 to another video signal suitable for driving a different kind of display monitor 22" at col. 5, line 27).

Regarding **claim 46**, Boehlke et al. discloses a system further comprising a memory to store the sampled image data ("decimator output matrix values Y(p,h) are stored at sequential addresses in memory 28" at col. 5, line 54).

10. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Boehlke et al. and Acharya as applied to claim 35 above, and further in view of Koselj et al.

The combination of Boehlke et al. and Acharya discloses a graphics display device as described in the 103 rejections above.

The Boehlke et al. and Acharya combination does not disclose the graphics display device including one or more LCD panels storing the sampled said image data in a memory.

Koselj et al. discloses a graphics display device (figure 18, numeral 8) including one or more LCD panels ("LCD display" at col. 21, line 48) for storing sampled image data ("new image data will be written into display memory, and during the next refresh

period (LCD timing control logic) this image will appear on the display" at col. 9, line 68) in a memory (figure 21, numeral 17).

It would have been obvious at the time the invention was made to one of ordinary skill in the art for the sampled image data of the Boehlke et al. and Acharya combination to be stored and displayed using the LCD taught by Koselj et al. as described above, to allow "high-level graphics commands travel between the CPU and the display part" (Koselj et al., at col. 3, line 27).

11. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Boehlke et al. and Acharya as applied to claim 37 above, and further in view of Crean et al.

The combination of Boehlke et al. and Acharya discloses an adding circuit adapted to begin a count sequence as described in the 103 rejections above.

The Boehlke et al. and Acharya combination does not disclose beginning said count sequence at an offset K.

Crean et al. discloses an image processing system beginning a count sequence ("functional requirements of sequencer 40 are that it be able to initialize at the beginning of a scan line, start at an offset location in memory representing an offset within the brick" at col. 6, line 31) at an offset K ("precomputed brick parameters (e.g., offset within the brick)" at col. 6, line 36; figure 1, letter S).

It would have been obvious at the time the invention was made to one of ordinary skill in the art for the count sequence of the Boehlke et al. and Acharya combination to be shifted using the offset taught by Crean et al. as described above, to "support the requirements of, for example, process controls, customer selection, and/or object optimized rendering" (Crean et al., at col.6, line 17).

Response to Arguments

Summary of Remarks (@ response page labeled 11): "Boehlke does not disclose a method of sampling or a sampling circuit".

Examiner's Response:.Disagreed. The decimator takes an input of pixels from the original image and accordingly outputs pixels that are based on a sampling of the input.

Summary of Remarks (@ response page labeled 11): "Boehlke does not disclose an increment of N-M.

Examiner's Response: In the previously stated case, N is 2 and M is 1, and N-M would therefore be 1. The count sequence is shown to be incremented in steps of 1.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Katrina Fujita whose telephone number is (571) 270-1574. The examiner can normally be reached on M-Th 8-5:30pm, F 8-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian P. Werner can be reached on (571) 272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KF

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BRIAN WERNER
SUPERVISORY PATENT EXAMINER